Listing of claims:

This listing of claims reflects the current listing. It is provided here for convenience only. No claims have been amended, added, or canceled in this Response.

Claim 1 (previously presented): A semiconductor device comprising:

a common substrate;

an SRAM device implemented on the common substrate and isolated by an STI isolation structure; and

a flash EPROM device implemented on the common substrate and isolated by a LOCOS isolation structure,

wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently.

Claims 2-3 (canceled)

Claim 4 (original): The semiconductor device according to claim 1 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

Claim 5 (previously presented): A system containing different types of isolation structures, the system comprising:

a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently;

an SRAM device on the first portion of the substrate; and

a flash EPROM device on the second portion of the substrate.

Claim 6 (original): The system according to claim 5 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

Claims 7-8 (canceled)

Claim 9 (previously presented): A semiconductor device comprising:

a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

Claim 10 (original): The semiconductor device according to claim 9 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

Claims 11-17 (previously canceled)

Claim 18 (previously presented): A semiconductor device, comprising:

a common substrate;

a first portion formed on the common substrate, the first portion comprising an SRAM device over a first single device layer, the first single device layer comprising a first active region and an STI isolation structure; and

a second portion formed on the common substrate, the second portion comprising a flash EPROM device over a second single device layer, the second single device layer comprising a second active region and a LOCOS isolation structure.

Claims 19-20 (canceled)

Claim 21 (previously presented): The semiconductor device of claim 18, wherein the first single device layer comprises an insulating oxide.

Claim 22 (previously presented): The semiconductor device of claim 18, wherein the second single device layer comprises an insulating oxide.

Claim 23 (previously presented): A semiconductor device comprising:

a common substrate;

an SRAM device implemented on the common substrate and formed over a first active region on a first isolated structure including an STI isolation structure; and

a flash EPROM device implemented on the common substrate and formed over a second active region on a second isolated structure including a LOCOS isolation structure, the second isolated structure having an outer portion extending a first depth into the substrate and an inner portion including the second active region and extending a second depth into the substrate, the first depth larger than the second depth.

Claim 24 (previously presented): The semiconductor device of claim 23, wherein the first isolated structure and the second isolated structure are contiguous.

Claim 25 (previously presented): The semiconductor device of claim 23, wherein the first isolated structure and the second isolated structure both comprise an oxide material.

Claim 26 (previously presented): A system containing a semiconductor device having a plurality of isolated structures, the system comprising:

a common substrate having a first area including an STI isolation structure and a second area including a LOCOS isolation structure, the second area having an outer portion extending a first depth into the substrate and an inner portion including an active region extending a second depth into the substrate, wherein the first depth is larger than the second depth;

an SRAM device implemented on the first area of the substrate; and

a flash EPROM device implemented on the second area of the substrate.

Claim 27 (previously presented): The system of claim 26, wherein the first area and the second area are contiguous.

Claim 28 (previously presented): The system of claim 27, wherein the first area and the second area both comprise an oxide material.